REMARKS/ARGUMENTS

Claim 15 and 18 have been amended. Claims 15-19 remain in the application. Support for the amendments to claims 15 and 18 can be found in Applicants' specification on page 8, lines 1-4 and in Figure 3.

I. SUMMARY OF THE JULY 16TH, 2003 OFFICE ACTION

Claims 15-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jeng U.S. Patent 5,821,621. The Office Action states that Jeng discloses a ***composite*** layer of low k silicon oxide dielectric material (22) on an oxide layer (12) of an integrated circuit. The Rejection goes on to say that the composite layer of low k silicon oxide dielectric material comprises a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties (22) and a second layer of low k silicon oxide dielectric material (24) to a desired thickness.

With respect to the rejection of claim 17, The Office Action states that Jeng discloses a composite layer of low k carbon doped silicon oxide (22, column 1, lines 45-55) exhibiting void-free deposition properties, comprising: a first layer of low k carbon-doped silicon oxide dielectric material exhibiting void-free deposition properties (22), and a second layer of carbon-doped low k silicon oxide dielectric material (24) by PECVD (column 4, lines 63-65).

II. THE JENG REFERENCE

Jeng U.S. Patent 5,821,621 discloses an improved method for integrating polymer and other low dielectric constant materials, which may have undesirable physical properties, into integrated circuit structures and processes, especially those requiring multiple levels of interconnect lines. Jeng combines the advantages of SiO_2 dielectric material with low dielectric constant materials by placing the low dielectric material only between tightly spaced apart lines. The inventor discusses the various types of undesirable capacitance which occur in integrated circuit structures, such as line to line capacitance and line to ground capacitance, and concludes that of those two types of capacitance, more than 90% is line to line capacitance. Jeng states that many polymeric materials have low dielectric constants, but also have a number of shortcomings with respect to at least their physical properties.

Jeng proposes to take advantage of the desirable low k characteristics of such polymeric dielectric materials by first spinning a low-k dielectric material across the surface of the wafer to fill the critical areas, i.e., the areas between closely spaced together interconnect lines. This also serves to fill all of the areas between all interconnect lines, i.e., the non-critical areas as well. The areas where the low-k material is to remain, are masked off with a resist mask. The unmasked low dielectric constant material in non-critical or widely spaced areas is then etched away, leaving the problematic but desirable low-k material in only those areas where needed, e.g., between closely spaced apart interconnect lines.

After removal of the resist mask, a layer of conventional dielectric material such as SiO_2 is applied over the entire structure, including the etched away areas, to fill the remaining area with SiO_2, e.g., to provide spacing between more widely spaced apart metal lines.

III. THE INVENTION

The invention claimed by Applicants is a composite low k dielectric layer comprising a first layer of low k silicon dioxide dielectric material formed on an oxide layer of an integrated circuit structure on a semiconductor substrate to fill the high aspect ratio space between closely spaced apart metal lines on the oxide layer. This first layer of low k dielectric material is formed of a low k dielectric material selected for its ability to form a void-free filling of the regions between closely space apart metal lines, i.e., selected for its ability to completely fill the high aspect ratio regions between such metal lines. This first low k dielectric layer is deposited until the resulting first layer of low k silicon oxide dielectric material reaches the level of the top of the metal lines on the oxide layer, completely filling the regions between the closely spaced apart metal lines.

The composite low k dielectric layer further includes a second layer of low k silicon oxide dielectric material, having a faster deposition rate than the first layer, which has been deposited over the first layer up to the desired overall thickness of the composite low k silicon oxide dielectric layer. In a preferred embodiment, the steps to form the resulting composite layer of low k silicon oxide dielectric material are all carried out in a single vacuum processing apparatus without removal of the substrate from the vacuum apparatus.

The resultant composite layer of low k silicon oxide dielectric materials exhibits void-free deposition properties in high aspect ratio regions between the closely spaced apart metal lines, and deposition rates in other regions comparable to standard k silicon oxide. This use of conventional low k dielectric material above the height of the metal lines results in reduced via poisoning characteristics, since vias pass through conventional low k dielectric material before reaching the tops of the metal lines.

IV. DISCUSSION

Claims 15-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jeng U.S. Patent 5,821,621. Applicants, in their previous response, argued that Jeng did not teach that his liner layer (22), used to inhibit interaction between his metal lines (14) and his dielectric materials, also possessed low k dielectric properties as well.

The Final Rejection acknowledged (and rejected) Applicants' arguments that they had been unable to find where Jeng taught that his liner layer (22), -- used to inhibit interaction between his metal lines (14) -- also possessed low k dielectric properties as well. The Office Action states that Applicants' point is moot for the following five reasons:

> 1. The instant claims fail to claim the dielectric constant or properties associated with a low k dielectric;
>
> 2. Jeng discloses in figs. 1-4 a low k silicon oxide dielectric layer (22);
>
> 3. It is well known in the art that silicon oxide is a low k dielectric;
>
> 4. The dielectric constant of silicon oxide is 3.8-4.2 which is considered low k dielectric material see Nalwa, Handbook of Low and High Dielectric Constant Materials and Their Applications, Vol. 1, pg. 66 (1999)); and
>
> 5. Jeng teaches that low k means a dielectric lower than 4.0. Therefore, since the method of Jeng teaches silicon oxide as the first layer, Jeng is inherently teaching low k dielectric because the values of the dielectric constant for silicon oxide are inherent to be in the art recognized range of lower than 4.0.

Applicants have now found a statement in Jeng that "The liner layer may be an etch-stopping layer such as a low-dielectric organic spin-on glass or silicon oxide." Applicants do not, therefore, intend to urge, at this time, the per se novelty of the use of two layers of low k dielectric material as an argument for patentability. However, since Applicants do intend to urge patentability of Applicants' composition based on the characteristics and positioning of

Applicants' individual layers, Applicants must respond to the five points listed in the Final Rejection.

With respect to the USPTO's first reason why arguing that liner layer (22) is a low k dielectric material is a moot point, each of Applicants' claims refer to a low k first layer and a low k second layer. The term "low k" is defined in Applicants' specification on page 6, lines 22-23. When a term is defined in a specification, use of that term in a claim imports that definition into the claim. Applicants' arguments are not moot for this reason.

The second reason is alleged to be that Jeng discloses in figs 1-4 a low k silicon oxide dielectric layer (22). There are no labels or other identifying words on any of the first four figures in Jeng, so one must refer back to the Jeng specification in which, at that time, Applicants had not been able to find any such identification of liner layer (22), nor had apparently the USPTO, since no column and line number for such a teaching has been furnished to Applicants by the USPTO.

Applicants must certainly challenge the third point of the USPTO that it is well known in the art that silicon oxide is a low k dielectric material. While such an allegation may be true in the general field of electronics in comparing, for example, the dielectric constant of silicon oxide with the dielectric constant of the dielectric materials in ceramic capacitors, such an allegation would have to be proven in the field of microelectronics by competent evidence before it could be established or accepted as known in the art that silicon oxide is a low k dielectric material.

With respect to the table from page 66 of the Nalwa handbook, which lists the dielectric constant of silicon to range from 3.8 to 4.2, Applicants are confused as to what such data proves. It appears that of the dielectric constants listed for 29 materials, only boron nitride has a higher dielectric constant value. How this supports a contention that conventional silicon oxide is a low k dielectric material is not apparent. (Note in this regard that the mere listing of silicon oxide with materials having lower dielectric properties does not make silicon oxide a low k

dielectric material.) Note also that the title of the Nalwa handbook reads " Handbook of Low ***and High*** Dielectric Constant Materials...". (emphasis added). Perhaps the inclusion of silicon oxide was to furnish an example of a high dielectric material.

Regarding the alleged Jeng definition of the term "low k", Applicants have defined this term in their specification on page 6, lines 22-23, and Applicants' definition is not at variance with art-accepted definitions for the term "low k".

Applicants' claims recite the presence of a first low k dielectric material having certain deposition characteristics (void-free in claims 15 and 18) or made of specific materials known to form void-free fillings (claims 17 and 19).

Furthermore, Applicants' ***first layer*** of low k dielectric material provides the ***void-free*** filler material. In constrast, it is obvious from Jeng's figures that if Jeng does provide any such void-free characteristics, it must be from layer 24 (his ***last*** low k layer).

Applicants claim that their second layer of low k dielectric material is formed over the tops of their metal lines and over their planarized first layer of low k dielectric material. There is no such planarized first layer of low k dielectric material over which a further layer of low k dielectric material is formed. Applicants have selected a first low k dielectric material known for its ability to form void-free coatings in high aspect regions and then Applicants have chosen a further low k dielectric material capable of providing a fast deposition rate to complete the formation of the low k dielectric material. No teaching of such discrimination has been found in the Jeng reference.

Both claims 17 and 19 specifically recite that the low k dielectric material used to form the low k material is the reaction product of a carbon-doped material and hydrogen peroxide. No such teaching or suggestion of the use of Applicants' specific void-free low k material have been found. In fact, it can be argued that Jeng actually argues against the use of Applicants' carbon-doped low k dielectric material, since Jeng states the following in the next sentence of column 1, after the cited lines 45-55):

> "Compared to SiO_2, these preferred low-k materials typically have ***low mechanical strength, poor dimensional stability, poor temperature stability, high moisture absorption and permeation, poor adhesion, large thermal expansion coefficient and an unstable stress level."*** (emphasis added)

Such comments by Jeng concerning the use of polymeric materials (which the USPTO apparently considers to be equivalent to "carbon-doped materials), does not encourage one skilled in the art to use such dielectric materials, but rather teach away from Applicants' invention.

Two further points should be noted with respect to any reliance on the newly cited Nalwa reference. First, a rejection under 35 U.S.C. 102 should be based on a single reference, not a combination of references. The need to rely on further references shows the failure of the original reference to teach the claimed invention.

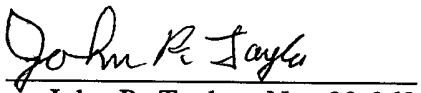
Further, in the instant case, the citation of a new reference in a Final Rejection, where the further rejection is not necessitated by any amendments to Applicants' claims, is at variance with the procedures laid out in MPEP 706.07(a).

V. **SUMMARY**

Applicants' claimed structure is not anticipated or suggested by the Jeng patent. Applicants' claims should be in condition for allowance.

If the Examiner in charge of this case feels that there are any remaining unresolved issues in this case, the Examiner is urged to call the undersigned attorney at the below listed telephone number which is in the Pacific Coast Time Zone.

Respectfully Submitted,



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